

METHOD AND APPARATUS FOR GENERATING A SEQUENCE OF CLOCK SIGNALS

TECHNICAL FIELD

5 This invention relates to generating a sequence of accurately phased clock signals, and more particularly, to using delay and phase locked loops to provide a sequence of clock signals that are accurately phased relative to a master clock signal.

BACKGROUND OF THE INVENTION

10 Clock signals are used by a wide variety of digital circuits to control the timing of various events occurring during the operation of the digital circuits. For example, clock signals are used to designate when commands and other signals used in computer systems are valid and can thus be used to control the operation of the computer system. A clock signal can then be used to latch
15 the command or other signals so that they can be used after the command or other signals are no longer valid.

 The problem of accurately controlling the timing of clock signals for high speed digital circuits is exemplified by clock signals used in high speed dynamic random access memories ("DRAMs") although the problem is, of course, also applicable to other digital circuits. Initially, DRAMs were
20 asynchronous and thus did not operate at the speed of an external clock. However, since asynchronous DRAMs often operated significantly slower than the clock frequency of processors that interfaced with the DRAM, "wait states" were often required to halt the processor until the DRAM had completed a
25 memory transfer. The operating speed of asynchronous DRAMs was successfully increased through such innovations as burst and page mode DRAMs which did not require that an address be provided to the DRAM for each memory

access. More recently, synchronous dynamic random access memories (“SDRAMs”) have been developed to allow the pipelined transfer of data at the clock speed of the motherboard. However, even SDRAMs are incapable of operating at the clock speed of currently available processors. Thus, SDRAMs cannot be connected directly to the processor bus, but instead must interface with the processor bus through a memory controller, bus bridge, or similar device. The disparity between the operating speed of the processor and the operating speed of SDRAMs continues to limit the speed at which processors may complete operations requiring access to system memory.

A solution to this operating speed disparity has been proposed in the form of a computer architecture known as “SyncLink.” In the SyncLink architecture, the system memory is coupled to the processor directly through the processor bus. Rather than requiring that separate address and control signals be provided to the system memory, SyncLink memory devices receive command packets that include both control and address information. The SyncLink memory device then outputs or receives data on a data bus that is coupled directly to the data bus portion of the processor bus.

An example of a packetized memory device using the SyncLink architecture is shown in Figure 1. The SyncLink memory device 10 includes a clock divider and delay circuit 40 that receives a master or command clock signal on line 42 and generates a large number of other clock and timing signals to control the timing of various operations in the memory device 10. The memory device 10 also includes a command buffer 46 and an address capture circuit 48 which receive an internal clock signal ICLK, a command packet CA0-CA9 on a command bus 50, and a FLAG signal on line 52. As explained above, the command packet contains control and address data for each memory transfer, and the FLAG signal identifies the start of a command packet which may include more than one 10-bit packet word. In fact, a command packet is generally in the

form of a sequence of 10-bit packet words on the 10-bit command bus 50. The command buffer 46 receives the command packet from the bus 50, and compares at least a portion of the command packet to identifying data from an ID register 56 to determine if the command packet is directed to the memory device 10 or some other memory device 10 in a computer system. If the command buffer determines that the command is directed to the memory device 10, it then provides a command word to a command decoder and sequencer 60. The command decoder and sequencer 60 generates a large number of internal control signals to control the operation of the memory device 10 during a memory transfer.

The address capture circuit 48 also receives the command words from the command bus 50 and outputs a 20-bit address corresponding to the address data in the command. The address is provided to an address sequencer 64 which generates a corresponding 3-bit bank address on bus 66, a 10-bit row address on bus 68, and a 7-bit column address on bus 70.

One of the problems of conventional DRAMs is their relatively low speed resulting from the time required to precharge and equilibrate circuitry in the DRAM array. The packetized memory device 10 shown in Figure 1 largely avoids this problem by using a plurality of memory banks 80, in this case eight memory banks 80a-h. After a memory read from one bank 80a, the bank 80a can be precharged while the remaining banks 80b-h are being accessed. Each of the memory banks 80a-h receive a row address from a respective row latch/decoder/driver 82a-h. All of the row latch/decoder/drivers 82a-h receive the same row address from a predecoder 84 which, in turn, receives a row address from either a row address register 86 or a refresh counter 88 as determined by a multiplexer 90. However, only one of the row latch/decoder/drivers 82a-h is active at any one time as determined by bank control logic 94 as a function of bank data from a bank address register 96.

The column address on bus 70 is applied to a column latch/decoder 100 which, in turn, supplies I/O gating signals to an I/O gating circuit 102. The I/O gating circuit 102 interfaces with columns of the memory banks 80a-h through sense amplifiers 104. Data is coupled to or from the memory banks 80a-h through the sense amplifiers 104 and I/O gating circuit 102 to a data path subsystem 108 which includes a read data path 110 and a write data path 112. The read data path 110 includes a read latch 120 receiving and storing data from the I/O gating circuit 102. In the memory device 10 shown in Figure 1, 64 bits of data are applied to and stored in the read latch 120. The read latch then provides four 16-bit data words to a multiplexer 122. The multiplexer 122 sequentially applies each of the 16-bit data words to a read FIFO buffer 124. Successive 16-bit data words are clocked through the FIFO buffer 124 by a clock signal generated from an internal clock by a programmable delay circuit 126. The FIFO buffer 124 sequentially applies the 16-bit words and two clock signals (a clock signal and a quadrature clock signal) to a driver circuit 128 which, in turn, applies the 16-bit data words to a data bus 130. The driver circuit 128 also applies the clock signals to a clock bus 132 so that a device, such as a processor, reading the data on the data bus 130 can be synchronized with the data.

The write data path 112 includes a receiver buffer 140 coupled to the data bus 130. The receiver buffer 140 sequentially applies 16-bit words from the data bus 130 to four input registers 142, each of which is selectively enabled by a signal from a clock generator circuit 144. Thus, the input registers 142 sequentially store four 16-bit data words and combine them into one 64-bit data word applied to a write FIFO buffer 148. The write FIFO buffer 148 is clocked by a signal from the clock generator 144 and an internal write clock WCLK to sequentially apply 64-bit write data to a write latch and driver 150. The write latch and driver 150 applies the 64-bit write data to one of the memory banks 80a-h through the I/O gating circuit 102 and the sense amplifier 104.

As mentioned above, an important goal of the SyncLink architecture is to allow data transfer between a processor and a memory device to occur at a significantly faster rate. However, the operating rate of a packetized DRAM, including the packetized memory device 10 shown in Figure 1, is limited by the time required to receive and process command packets applied to the memory device 10. More specifically, not only must the command packets be received and stored, but they must also be decoded and used to generate a wide variety of signals. However, in order for the memory device 10 to operate at a very high speed, the command packets must be applied to the memory device 10 at a correspondingly high speed. As the operating speed of the memory device 10 increases, the command packets are provided to the memory device 10 at a rate that can exceed the rate at which the command buffer 46 can process or even store the command packets.

One of the limiting factors in the speed at which the command buffer 46 can store and process the command packets is control of the relative timing between the command packets and the clock signal ICLK. Both the command data signals and the ICLK signal are delayed relative to receipt of the command packet on the command bus 50 and the master clock signal on line 42. Furthermore, the amount of the delay is highly variable, and it is difficult to control. If the delay of the internal clock signal ICLK cannot be precisely controlled, it may cause the latch in the command buffer 48 to latch invalid command data signals. Thus, the speed at which command packets can be applied to the memory device 10 is limited by the delays in the memory device 10. Similar problems exist for other control signals in the memory device 10 which control the operation of the memory device 10 during each clock cycle.

Although the foregoing discussion is directed to the need for faster command buffers in packetized DRAMs, similar problems exist in other memory devices, such as asynchronous DRAMs and synchronous DRAMs, which must

process control and other signals at a high rate of speed. Thus, for the reasons explained above, the limited operating speed of conventional command buffers threatens to severely limit the maximum operating speed of memory devices, particularly packetized DRAMs. Therefore, there is a need to precisely control the timing of clock signals relative to other signals, such as command packets applied to a command buffer in a packetized DRAM.

SUMMARY OF THE INVENTION

A clock generator circuit is used to provide a sequence of clock signals that have predetermined phases relative to a master clock signal. The clock generator circuit includes a first locked loop generating the sequence of clock signals which are increasingly delayed from a first clock signal to a last clock signal. Two of the clock signals, preferably the first and last clock signals, are locked to each other, such as by using a delay-locked loop, so that they have a predetermined phase with respect to each other. A second lock loop, which may also be a delay-locked loop, locks one of the clock signals in the sequence to the master clock signal so that the clock signals have respective phases with respect to the master clock signal. Where delay-locked loops are used, the first delay lock loop delay may lock the first clock signal and the last clock signal so that they are the inverse of each other. As a result, the first and last clock signals have respective phases that are 180 degrees from each other. Similarly, the second delay-lock loop may delay lock the first clock signals to the master clock signal so that they have substantially the same phase. The first delay-locked loop preferably includes a first voltage controlled delay circuit and a first phase detector. The first voltage controlled delay circuit generates the sequence of clock signals from the reference clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal. A first phase detector compares the phase of the first and last clock signals and

generates the first control signal as a function of the difference therebetween. Likewise, the second delay-locked loop preferably includes a second voltage controlled delay circuit and a second phase detector. The second voltage controlled delay circuit receives the master clock signal and generates a reference
 5 clock signal having a delay relative to the master clock signal that is a function of a second control signal. The second phase detector compares the phase of the master clock signal to the phase of the first clock signal and generating the second control signal as a function of the difference therebetween. A multiplexer may be coupled to the first delay-lock loop to couple one of the clock signals to a
 10 clock output terminal for use, for example, to latch command data in packetized DRAM.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a conventional packetized dynamic random access memory ("DRAM") that may use a clock generator in accordance
 15 with an embodiment of the present invention.

Figure 2 is a block diagram illustrating the manner in which an embodiment of clock generator in accordance with present invention may be used in a command latch in the packetized DRAM of Figure 1.

Figure 3 is a more detailed block diagram and logic diagram of the
 20 command latch of Figure 2 using an embodiment of a clock generator in accordance with present invention.

Figure 4 is a timing diagram showing many of the waveforms present in the command latch of Figure 3.

Figure 5 is a block diagram of a computer system using a plurality
 25 of DRAMs, each of which include the command latch of Figure 3.

DETAILED DESCRIPTION OF THE INVENTION

One embodiment of a command latch 200 using an embodiment of a clock generator 210 in accordance with present invention is illustrated in Figure 2. The command latch 200 also includes a latch circuit 212 receiving a
 5 command data bit CMD DATA from a command packet on a line of the command bus 50. The clock generator 210 receives a master or command clock signal CMD CLK on line 42 and generates the internal clock signal ICLK which is applied to the clock input of the latch circuit 212. The output of the latch circuit 212 is coupled to a variety of circuits in the memory device 10, including
 10 a select circuit 214. As explained below, the clock generator 210 produces a sequence of clock signals each having an increased delay relative to the leading edge of the master clock. One of the clock signals in the sequence is selected for use as the internal clock signal ICLK for clocking the latch circuit 212. The clock signal in the sequence for use as ICLK is selected by a multi-bit select
 15 word SELECT generated by the select circuit 214. Basically, the select circuit 214 determines which of the clock signals in the sequence has the proper timing to match the delay of the command data from the command bus 50 to the input of the latch circuit 212. The select circuit 214 then applies an appropriate SELECT word to the clock generator 210 to use the selected clock signal in the sequence
 20 as the internal clock signal ICLK.

A variety of designs may be used for the select circuit 214, as will be apparent to one skilled in the art. For example, a plurality of very short logic “1” pulses may be applied to the command bus line 50 in synchronism with the command clock signal CMD CLK. The select circuit 214 can then select each of
 25 the clock signals in the sequence and determine which clock signal(s) are able to capture the logic “1” pulses. If several clock signals are successful in capturing the logic “1” pulses, then the clock signal occurring midway between the successful clock signals can be used as the internal clock signal ICLK.

The command latch 200, including one embodiment of a clock generator 210 in accordance with the present invention, is shown in greater detail in Figure 3. The latch 212 is illustrated in Figure 3 as consisting of a receiver buffer 240 receiving a respective one of 10 bits of the command data CMD DATA. The output of the receiver buffer 240 is applied to the data input D of a latch circuit 242. The latch circuit 242 latches or stores the logic level applied to its D input whenever a clock signal applied to its clock C input goes high. The stored logic level is then continuously applied to the output of the latch circuit 242. Although a single receiver buffer 240 and latch circuit 242 are shown in Figure 3, it will be understood that there are actually 10 receiver buffers 240 and latch circuits 242 to store the 10 bits of the command data on the command bus 50.

As explained above, it is very difficult to clock the latch circuit 242 at the proper time at the maximum speed of the command latch 200 because delays of the CMD DATA from the command bus 50 to the latch circuit 242 may not be equal to delays of the CMD CLK from the line 42 to the clock input of the latch circuit 242. Also, of course, unequal delays external to an integrated circuit containing the command latch 200 may cause the CMD CLK and the CMD DATA to be applied to the integrated circuit at different times. The function of the clock generator 210 is to provide an internal clock signal ICLK to the clock input of the latch circuit 242 that is capable of storing a command data bit at even the fastest operating speed of the command latch 200 despite any unequal internal or external delays that would cause the command bit and ICLK to be coupled to the latch circuit 242 at different times. However, it will be understood that the clock generator 210 may be used for other purposes both in dynamic random access memories and in other circuits.

The master or command clock CMD CLK is coupled from line 42 through a receiver buffer 250 substantially identical to the receiver buffer 240

coupling a command data bit to the latch circuit 242. The output of the receiver buffer 250 is applied to a conventional voltage controlled delay circuit 252 and to one input of a phase detector 254. The voltage controlled delay circuit 252 couples the output of the receiver buffer 250 to an output line 256 with a delay that is a function of a control signal applied to the delay circuit 252 on line 258. Although the control signal on line 258 is an analog voltage, it will be understood that other types of control signals, including digital words, may alternatively be used. The output of the voltage controlled delay circuit 252 is applied to a multi-tap voltage controlled delay line 260.

The multi-tap voltage controlled delay line 260 couples the clock signal applied to its input on line 256 to a plurality of output lines 264a-264n. The incoming clock signal is coupled to the output lines 264 with an increasing delay from the first line 264a to the last line 264n. In the embodiment illustrated in Figure 3, there are 17 output lines 264, but the delay line 260 may have a greater or lesser number of output lines 264. When a delay locked loop that includes the delay line 260 is locked as explained below, the signals at the first output line 264a and the last or 17th output line 264n are the inverse of each other, *i.e.*, phased 180 degrees from each other. Thus, the signals on the 17 lines are delayed by 11.25 degrees more than the signal coupled to the previous line 264. Thus, the first line 264a has a relative phase of zero degrees, the 16th line 264n-1 has a phase of 168.75 degrees and the last line 264n has a phase of 180 degrees. More specifically, a control voltage applied to the delay line 260 through line 270 is adjusted so that the phase of the signal on the last line 264n relative to the phase on the first line 264a is 180 degrees. This is accomplished by applying the first line 264a and the last line 264n to respective inputs of a phase detector 272.

As mentioned above, the delay line 260 and phase detector 272 implement a first delay locked loop. When the first delay locked loop is locked,

the signal on line 264n will have a phase relative to the phase of the signal on line 264a of 180 degrees. Therefore, as mentioned above, the signal on each of the output lines 264a-264n will sequentially increase from zero degrees to 180 degrees. Although the signals on lines 264a-n are equally phased apart from each other, it will be understood that equal phasing is not required.

The clock generator 210 also includes a second delay locked loop formed by the phase detector 254, the voltage controlled delay circuit 252 and the voltage controlled delay line 260. More particularly, the last output line 264n of the delay line 260 is applied through a simulated multiplexer circuit 290 and a clock driver 292 to one input of the phase detector 254. It will be recalled that the other input of the phase detector 254 receives the output of the receiver buffer 250. Like the phase detector 272, when the second delay locked loop is locked, the signals applied to the phase detector 254 are the inverse of each other. Thus, when the second loop is locked, the phase of the signal at the output of the clock driver 292 is 540 degrees (effectively 180 degrees) relative to the phase of the signal at the output of the receiver buffer 250.

The remaining output lines 264a-264n-1 of the delay line 260 are coupled to a multiplexer 310 having a plurality of output lines coupled to respective clock drivers 312a-n. The multiplexer 310 couples the input of each of the clock drivers 312a-n to any one of the output lines 264a-264n-1 as determined by respective select words SELECT. The clock driver 312a is used to generate the internal clock signal ICLK which is coupled to the clock input of the latch circuit 242. The other clock drivers 312b-n are used to couple various clock outputs from the delay line to other circuits in the memory device (not shown).

The phase detectors 254, 272 are each implemented using to a phase detector circuit 330, a charge pump 332 and a capacitor 334. However, other varieties of phase detectors may alternatively be used.

The phase detector circuit 330 applies either an increase signal on line 336 or a decrease signal on line 338 to respective inputs of the charge pump 332. The phase detector circuit 330 generates the increase signal on line 336 whenever the phase of a first signal on one of its inputs relative to a second signal on the other of its inputs is less than 180 degrees. As explained below, the increase signal on line 336 causes the charge pump 332 to adjust the control voltage to increase the delay of the first signal so that the phase of the first signal relative to the phase of the second signal approaches 180 degrees. The phase detector circuit 330 generates the decrease signal on line 338, in the opposite condition, *i.e.*, when the phase of the second signal relative to the first signal is greater than 180 degrees. The decrease signal on line 338 causes the charge pump 332 to adjust the control voltage to reduce the delay of second signal toward 180 degrees.

Although the phase detector circuit 330 may be implemented in a variety of ways, it may simply use two set-reset flip-flops (not shown) for generating the increase and decrease signals, respectively. The increase flip-flop is set by the rising edge of the first signal on one of the inputs and reset by the falling edge of the second signal on the other input. Thus, the duration that the flip-flop is set, and hence the duration of the increase signal on line 336, corresponds to the period of time that the second signal must be further delayed to have a phase of 180 degrees relative to the phase of the first signal. Similarly, the flip-flop producing the decrease signal on line 338 is set by the falling edge of the second signal and reset by the rising edge of the first signal so that the duration of the decrease signal on line 338 corresponds to the time that the second signal is delayed beyond the time that it would have a phase of 180 degrees relative to the phase of the first signal.

There are also a variety of approaches for implementing the charge pump 332. However, the charge pump 332 can be implemented by simply

applying a constant current to the capacitor 334 for the duration of each increase signal on line 336 and removing a constant current from the capacitor 334 for the duration of each decrease signal on line 338. Appropriate circuitry could also be included in either the phase detector circuit 330 or the charge pump 332 to provide hysteresis in a band when the first and second signals have relative phases of approximately 180 degrees from each other as will be apparent to one skilled in the art. The operation of the command latch 200 of Figure 3 can best be explained with reference to the timing diagram of Figure 4. As illustrated in Figure 4, the command clock signal CMD CLK on line 42 is delayed by approximately 70 degrees in passing through the receiver buffer 250 to node A (Figure 3). Assuming that both of the delay-lock loops are locked, the signal at the output of the receiver buffer 250 is delayed by 120 degrees in passing through the voltage controlled delay circuit 252 to node B. The signal on node B is then coupled to node C with a delay of another 120 degrees and to node D with a delay of 300 degrees so that the signals at nodes C and D are phased 180 degrees apart from each other. Since the signals at nodes C and D are compared to each other by the phase detector 272, the phase detector 272 adjusts the control voltage on line 270 to ensure that the signals at nodes C and D are phased 180 degrees from each other. The other outputs from the delay line 260 have phases relative to the phase of the signal at node C that increase 11.25 degrees for each output in sequence from the first line 264a to the last line 264n.

As mentioned above, one of the first 16 output lines 264a-264n-1 of the delay lines 260 is coupled through the multiplexer 310 and the clock driver 312a to provide the internal clock signal ICLK at node E. In passing through the multiplexer 310 and the clock driver 312a, the selected output from the delay line is delayed by another 120 degrees. Thus, the signal E₀ coupled from the first output line of the delay line 260 is delayed by 120 degrees, the signal E₄ from the fifth output is delayed by 165 degrees, the signal E₈ from the ninth output is

delayed by 210 degrees, the signal E12 from the 13th output is delayed by 255
 degrees, and the signal E15 from the 16th output is delayed by 288.75 degrees.
 Although the output signals are coupled from the delay line 260 through the
 multiplexer 310 and clock driver 312a with a delay, that delay is matched by the
 5 coupling of the signal from line 264n through the simulated multiplexer 290 and
 clock driver 292 since the same circuit is used for the simulated multiplexer 290
 as the multiplexer 310 and the clock driver 292 is identical to the clock driver
 312a. For this reason, and because the phase of the signal on line 264n is 180
 degrees relative to the phase of the signal on line 264a, the signal at the output of
 10 the clock driver 292 at node G has a phase relative to the phase of the signal Eo
 at the output of the clock 312a of 180 degrees. Since the signals applied to the
 inputs of the phase detector 254 are the inverse of each other when the delay-
 locked loop is locked, the signal Eo has substantially the same phase as the signal
 at the output of the receiver buffer 250. Furthermore, the delay of the voltage
 15 controlled delay circuit 252 will be adjusted so that the signal Eo always has the
 same phase as the command clock coupled to the output of the receiver buffer
 250 at A. Assuming the CMD DATA is valid on the rising edge of the CMD
 CLK signal, the command data bit coupled to the latch circuit 242 is valid on the
 rising edge of ICLK since ICLK is properly phased to the signal at node A and
 20 the delay through the receiver buffer 250 is substantially the same as the delay
 through the receiver buffer 240.

In operation, the multiplexer 310 selects one of the outputs from
 the delay line 260 as determined by the SELECT signal so that the optimum
 clock signal between Eo and E15 (Figure 4) will be used as the internal clock
 25 ICLK.

In summary, the "inner" delay locked loop formed by the phase
 detector 272 and the voltage controlled delay circuit 260 generates a sequence of
 signals that have increasing phases from zero to 180 degrees. The "outer" delay

locked loop formed by the phase detector 254, the voltage controlled delay circuit 252 and the delay line 260 align one of the clock signals in the sequence to the command clock. As a result, all of the clock signals at the output of the delay line 260 have respective predetermined phases relative to the phase of the command clock at node A.

Although the embodiment of the clock generator 210 illustrated in Figure 3 uses delay-locked loops, it will be understood that other locked loop circuits, such as phase-locked loop circuits, may also be used. Other modifications will also be apparent to one skilled in the art.

A computer system using the command latch 200 of Figures 2 and 3 in each of a plurality of packetized DRAMs 10 of Figure 1 is shown in Figure 5. With reference to Figure 5 the computer system 400 includes a processor 402 having a processor bus 404 coupled to three packetized dynamic random access memory or SyncLink DRAMs ("SLDRAM") 10a-c. The computer system 400 also includes one or more input devices 4100, such as a keypad or a mouse, coupled to the processor 402 through a bus bridge 412 and an expansion bus 414, such as an industry standard architecture ("ISA") bus or a Peripheral component interconnect ("PCI") bus. The input devices 410 allow an operator or an electronic device to input data to the computer system 400. One or more output devices 420 are coupled to the processor 402 to display or otherwise output data generated by the processor 402. The output devices 420 are coupled to the processor 402 through the expansion bus 414, bus bridge 412 and processor bus 404. Examples of output devices 420 include printers and video display units. One or more data storage devices 422 are coupled to the processor 402 through the processor bus 404, bus bridge 412, and expansion bus 414 to store data in or retrieve data from storage media (not shown). Examples of storage devices 422 and storage media include fixed disk drives floppy disk drives, tape cassettes and compact-disk read-only memory drives.

In operation, the processor 402 communicates with the memory devices 10a-c via the processor bus 404 by sending the memory devices 10a-c command packets that contain both control and address information. Data is coupled between the processor 402 and the memory devices 10a-c, through a data bus portion of the processor bus 404. Although all the memory devices 10a-c are coupled to the same conductors of the processor bus 404, only one memory device 10a-c at a time reads or writes data, thus avoiding bus contention on the processor bus 404. Bus contention is avoided by each of the memory devices 10a-c and the bus bridge 412 having a unique identifier, and the command packet contains an identifying code that selects only one of these components.

The computer system 400 also includes a number of other components and signal lines which have been omitted from Figure 5 in the interests of brevity. For example, as explained above, the memory devices 10a-c also receive a command or master clock signal to provide internal timing signals, a data clock signal clocking data into and out of the memory device 16, and a FLAG signal signifying the start of a command packet.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.